



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/615,042	07/08/2003	Valeriy Sukharev	03-0509	3892
24319	7590	02/08/2005	EXAMINER	
LSI LOGIC CORPORATION			FENTY, JESSE A	
1621 BARBER LANE			ART UNIT	PAPER NUMBER
MS: D-106			2815	
MILPITAS, CA 95035				

DATE MAILED: 02/08/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	Application No.	Applicant(s)
	10/615,042	SUKHAREV ET AL.
	Examiner Jesse A. Fenty	Art Unit 2815

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
Period for Reply

**A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM  
THE MAILING DATE OF THIS COMMUNICATION.**

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) Responsive to communication(s) filed on 03 December 2004.
- 2a) This action is **FINAL**.                            2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) Claim(s) 1-14 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) Claim(s) \_\_\_\_\_ is/are allowed.
- 6) Claim(s) 1-14 is/are rejected.
- 7) Claim(s) \_\_\_\_\_ is/are objected to.
- 8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on \_\_\_\_\_ is/are: a) accepted or b) objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a) All    b) Some \* c) None of:  
1. Certified copies of the priority documents have been received.  
2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)	4) <input type="checkbox"/> Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)	5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)
3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____ .	6) <input type="checkbox"/> Other: _____ .

## DETAILED ACTION

### *Claim Rejections - 35 USC § 112*

1. The rejection based on the first paragraph of 35 U.S.C. 112 is withdrawn.

### *Claim Rejections - 35 USC § 102*

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-14 are rejected under 35 U.S.C. 102(b) as being anticipated by McTeer (U.S. Patent No. 6,204,179 B1).

In re claim 1, McTeer discloses a method of forming an interconnect in a substrate which includes one or more dielectric layers and a copper deposit, said method comprising:

forming a trench in the substrate (column 17, lines 8-10); forming a via in the substrate to the copper deposit; depositing an interconnect liner layer (6) of aluminum-copper alloy comprised primarily of Aluminum in the trench and via; depositing copper onto the aluminum-copper alloy interconnect liner layer (column 21, lines 20-26); and polishing the copper (column 20, lines 24-28), wherein the interconnect liner layer is a permanent component of the interconnect and does not interact with the copper or copper deposit to form an alloy at any time while the method is performed.

In re claim 2, McTeer discloses the method of claim 1, wherein the step of depositing a layer of aluminum-copper alloy comprises depositing aluminum – 0.5% copper alloy using a PVD technique (column 18, lines 15-27).

In re claim 3, McTeer discloses a method of forming an interconnect in a substrate which includes one or more dielectric layers and a copper deposit, said method comprising:

Forming a trench in the substrate (column 17, lines 8-10); forming a via in the substrate to the copper deposit; depositing an intermediate liner layer (4) in the trench and via and on the copper deposit; depositing an interconnect liner layer (6) of aluminum-copper alloy comprised primarily of Aluminum on the intermediate layer (column 21, lines 20-26); depositing copper into the aluminum-copper alloy; and polishing the copper (column 20, lines 24-28), wherein the interconnect liner layer is a permanent component of the interconnect and does not interact with the copper or copper deposit to form an alloy at any time while the method is performed.

In re claim 4, McTeer discloses the method of claim 3, wherein the step of depositing a layer of aluminum-copper alloy comprises depositing aluminum – 0.5% copper alloy using a PVD technique (column 18, lines 15-27).

In re claim 5, McTeer discloses the method of claim 3, wherein the step of depositing an intermediate liner layer comprises depositing TaN (column 17, lines 62-65; column 18, lines 1-3).

In re claim 11, McTeer discloses the method of claim 1, further comprising depositing the interconnect layer such that said interconnect layer is in contact with the copper deposit (3).

In re claim 12, McTeer discloses the method of claim 1, wherein the step of depositing the interconnect liner layer comprises depositing a layer of aluminum – 0.5% copper alloy.

In re claim 13, McTeer discloses the method of claim 3, wherein the step of depositing the interconnect liner layer comprises depositing a layer of aluminum – 0.5% copper alloy.

In re claim 6, McTeer (Fig. 11) discloses an interconnect in a substrate which includes one or more dielectric layers, said interconnect comprising a first copper deposit (15), a second copper deposit (3), and an aluminum-copper alloy interconnect liner (6) comprised primarily of Aluminum (column 18, lines 16-18) disposed between and in (electrical) contact with the first and second copper deposits and between the second copper deposit (3) and at least one of the dielectric layers (14), wherein the interconnect liner is a permanent component of the interconnect and is not combined with either of the copper deposits to form an alloy.

In re claim 7, McTeer discloses the device of claim 6. The limitation, “wherein the ... has been deposited using a PVD technique,” refers to the process for making this product. Applicant is reminded that a Aproduct by process $\equiv$  claim is directed to the product per se, no matter how actually made, *In re Hirao*, 190 USPQ 15 at 17 (footnote 3). See also *In re Brown*, 173 USPQ 685; *In re Luck*, 177 USPQ 523; *In re Fessmann*, 180 USPQ 324; *In re Avery*, 186 USPQ 161; *In re Wertheim*, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); *In re Marosi* et al, 218 USPQ 289; and particularly *In re Thorpe*, 227 USPQ 964, all of which make it clear that it is the patentability of the final product per se which must be determined in a Aproduct by process $\equiv$  claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in Aproduct by process $\equiv$  claims or not. Note that applicant has the burden of proof in such cases, as the

above caselaw makes clear. Therefore, since McTeer disclose the aluminum-copper alloy structure in the same manner as the claimed structure, the prior art meets the claim.

In re claim 8, as best understood, McTeer (Fig. 11) discloses a semiconductor device comprising:

An interconnect in a substrate which includes one or more dielectric layers, said interconnect comprising a first copper deposit (15), a second copper deposit (3), an intermediate interconnect liner (4) and disposed between the first and second copper deposits and in contact with the first copper deposit (15); and an aluminum-copper alloy (6) interconnect liner disposed between the first and second copper deposits between the second copper deposit and at least one of the dielectric layers, and in contact with the second copper deposit (3), wherein the interconnect liner is a permanent component of the interconnect and is not combined with either of the copper deposits to form an alloy.

In re claim 9, McTeer discloses the device of claim 8. The limitation, “wherein the ... has been deposited using a PVD technique,” refers to the process for making this product and is not given patentable weight regarding the structure of this claim. See above.

In re claim 10, McTeer discloses the device of claim 8, wherein the intermediate interconnect liner comprises TaN (column 17, lines 62-64).

In re claim 14, McTeer discloses the device of claim 8, wherein said aluminum-copper alloy interconnect liner comprises a layer of aluminum – 0.5% copper alloy.

***Claim Rejections - 35 USC § 103***

3. Claims 1-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over McTeer (as above) in view of Hsu et al. (U.S. Patent No. 6,150,252).

In re claim 1, McTeer discloses a method of forming an interconnect in a substrate which includes one or more dielectric layers and a copper deposit, said method comprising:

forming a trench in the substrate (McTeer, column 17, lines 8-10); forming a via in the substrate to the copper deposit; depositing an interconnect liner layer (6) of aluminum-copper alloy comprised primarily of Aluminum in the trench and via; depositing copper onto the aluminum-copper alloy interconnect liner layer (McTeer, column 21, lines 20-26); and polishing the copper (column 20, lines 24-28).

If McTeer is not interpreted to provide a method wherein the interconnect liner layer is a permanent component of the interconnect and does not interact with copper or copper deposit to form an alloy at any time while the method is performed, said liner layer is disclosed by Hsu. Hsu (esp. Fig. 3B) discloses a method of depositing an interconnect liner layer (46') comprising primarily aluminum (McTeer, column 7, lines 58-59) as a permanent component. It would have been obvious for one skilled in the art at the time of the invention to deposit a liner layer at low temperature as disclosed by Hsu for the device of McTeer for the purpose, for example, of permitting for higher conformity metal deposition within the cavity (Hsu; column 8, lines 19-23).

In re claim 2, McTeer in view of Hsu discloses the method of claim 1, wherein the step of depositing a layer of aluminum-copper alloy comprises depositing aluminum – 0.5% copper alloy using a PVD technique (McTeer, column 18, lines 15-27).

In re claim 3, McTeer discloses a method of forming an interconnect in a substrate which includes one or more dielectric layers and a copper deposit, said method comprising:

Forming a trench in the substrate (McTeer, column 17, lines 8-10); forming a via in the substrate to the copper deposit; depositing an intermediate liner layer (4) in the trench and via and on the copper deposit; depositing an interconnect liner layer (6) of aluminum-copper alloy comprised primarily of Aluminum on the intermediate layer (McTeer, column 21, lines 20-26); depositing copper into the aluminum-copper alloy; and polishing the copper (McTeer, column 20, lines 24-28).

If McTeer is not interpreted to provide a method wherein the interconnect liner layer is a permanent component of the interconnect and does not interact with copper or copper deposit to form an alloy at any time while the method is performed, said liner layer is disclosed by Hsu. Hsu (esp. Fig. 3B) discloses a method of depositing an interconnect liner layer (46') comprising primarily aluminum (column 7, lines 58-59) as a permanent component. It would have been obvious for one skilled in the art at the time of the invention to deposit a liner layer at low temperature as disclosed by Hsu for the device of McTeer for the purpose, for example, of permitting for higher conformity metal deposition within the cavity (Hsu; column 8, lines 19-23).

In re claim 4, McTeer in view of Hsu discloses the method of claim 3, wherein the step of depositing a layer of aluminum-copper alloy comprises depositing aluminum – 0.5% copper alloy using a PVD technique (McTeer, column 18, lines 15-27).

In re claim 5, McTeer in view of Hsu discloses the method of claim 3, wherein the step of depositing an intermediate liner layer comprises depositing TaN (McTeer, column 17, lines 62-65; column 18, lines 1-3).

In re claim 11, McTeer in view of Hsu discloses the method of claim 1, further comprising depositing the interconnect layer such that said interconnect layer is in contact with the copper deposit (3).

In re claim 12, McTeer in view of Hsu discloses the method of claim 1, wherein the step of depositing the interconnect liner layer comprises depositing a layer of aluminum – 0.5% copper alloy.

In re claim 13, McTeer in view of Hsu discloses the method of claim 3, wherein the step of depositing the interconnect liner layer comprises depositing a layer of aluminum – 0.5% copper alloy.

In re claim 6, McTeer (Fig. 11) discloses an interconnect in a substrate which includes one or more dielectric layers, said interconnect comprising a first copper deposit (15), a second copper deposit (3), and an aluminum-copper alloy interconnect liner (6) comprised primarily of Aluminum (column 18, lines 16-18) disposed between and in (electrical) contact with the first and second copper deposits and between the second copper deposit (3) and at least one of the dielectric layers (14).

If McTeer is not interpreted to provide the structure wherein the interconnect liner is a permanent component of the interconnect and is not combined with either of the copper deposits to form an alloy, said liner layer is disclosed by Hsu. Hsu (esp. Fig. 3B) discloses an interconnect liner layer (46') comprising primarily aluminum (column 7, lines 58-59) as a permanent component. It would have been obvious for one skilled in the art at the time of the invention to deposit a liner layer as disclosed by Hsu for the device of McTeer for the purpose,

for example, of permitting for higher conformity metal deposition within the cavity (Hsu; column 8, lines 19-23).

In re claim 7, McTeer in view of Hsu discloses the device of claim 6. The limitation, “wherein the ... has been deposited using a PVD technique,” refers to the process for making this product. Applicant is reminded that a Aproduct by process $\equiv$  claim is directed to the product per se, no matter how actually made, *In re Hirao*, 190 USPQ 15 at 17 (footnote 3). See also *In re Brown*, 173 USPQ 685; *In re Luck*, 177 USPQ 523; *In re Fessmann*, 180 USPQ 324; *In re Avery*, 186 USPQ 161; *In re Wertheim*, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); *In re Marosi* et al, 218 USPQ 289; and particularly *In re Thorpe*, 227 USPQ 964, all of which make it clear that it is the patentability of the final product per se which must be determined in a Aproduct by process $\equiv$  claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in Aproduct by process $\equiv$  claims or not. Note that applicant has the burden of proof in such cases, as the above caselaw makes clear. Therefore, since McTeer disclose the aluminum-copper alloy structure in the same manner as the claimed structure, the prior art meets the claim.

In re claim 8, McTeer (Fig. 11) discloses a semiconductor device comprising:

An interconnect in a substrate which includes one or more dielectric layers, said interconnect comprising a first copper deposit (15), a second copper deposit (3), an intermediate interconnect liner (4) and disposed between the first and second copper deposits and in contact with the first copper deposit (15); and an aluminum-copper alloy (6) interconnect liner disposed between the first and second copper deposits between the second copper deposit and at least one of the dielectric layers, and in contact with the second copper deposit (3).

If McTeer is not interpreted to provide the structure wherein the interconnect liner is a permanent component of the interconnect and is not combined with either of the copper deposits to form an alloy, said liner layer is disclosed by Hsu. Hsu (esp. Fig. 3B) discloses an interconnect liner layer (46') comprising primarily aluminum (column 7, lines 58-59) as a permanent component. It would have been obvious for one skilled in the art at the time of the invention to deposit a liner layer as disclosed by Hsu for the device of McTeer for the purpose, for example, of permitting for higher conformity metal deposition within the cavity (Hsu; column 8, lines 19-23).

In re claim 9, McTeer in view of Hsu discloses the device of claim 8. The limitation, “wherein the ... has been deposited using a PVD technique,” refers to the process for making this product and is not given patentable weight regarding the structure of this claim. See above.

In re claim 10, McTeer in view of Hsu discloses the device of claim 8, wherein the intermediate interconnect liner comprises TaN (McTeer, column 17, lines 62-64).

In re claim 14, McTeer in view of Hsu discloses the device of claim 8, wherein said aluminum-copper alloy interconnect liner comprises a layer of aluminum – 0.5% copper alloy.

#### *Response to Arguments*

4. Applicant's arguments filed 12/03/04 have been fully considered but they are not persuasive. Applicant's amendment filed 12/03/03 is an attempt to distinguish the instant claims over the cited prior art of McTeer. However, the new claim language is not sufficient in that regard.

a. Regarding the 35 USC 102 rejection over McTeer ('179), the claim language does not clearly distinguish over the prior art. In McTeer ('179), the interconnect liner layer

(6) in its final (permanent) form comprises an aluminum-copper alloy primarily of aluminum, as claimed. The amended claim attempts to distinguish the application's liner layer by calling said layer a "permanent component" and suggesting that said liner layer "does not interact with the copper or copper deposit to form an alloy at any time while the method is performed." A careful analysis of these words shows that the art of McTeer is still valid.

i. For starters, the liner layer itself is an aluminum-copper alloy, as claimed. The description "permanent component" does not work to define when the alloy layer becomes or does not become permanent. The alloy formed by McTeer after anneal and reflow can be interpreted as a "permanent component" because the layer is formed and does not move out of position at any time after being formed.

ii. The second phrase, "... and does not interact with the copper or copper deposit to form an alloy at any time while the method is performed" is not entirely clear. The interconnect liner layer as claimed and the interconnect liner layer (6) of McTeer are both aluminum-copper alloys. The new claim language directs that the alloy liner layer should not further interact with copper to form an alloy.

McTeer does not disclose the aluminum-copper alloy further interacting with the copper to form another alloy. True that the aluminum layer (5) of McTeer combines with a first copper deposit to form an alloy (6), but the aluminum layer by itself, is not the claimed aluminum-copper liner layer. Thus, the liner layer (6) of McTeer does not further interact with copper and the amended claim does not distinguish over the prior art of McTeer.

b. Secondly, if applicant does not think the McTeer reference reads on the claims as written, a secondary reference, Hsu ('252), and rejection are provided with give a second interpretation of what is known in the art.

***Conclusion***

5. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

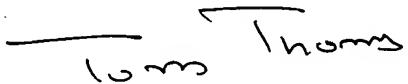
A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jesse A. Fenty whose telephone number is 571-272-1729. The examiner can normally be reached on 5/4-9 1st Fri. Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 571-272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jesse A. Fenty  
Examiner  
Art Unit 2815

  
TOM THOMAS  
SUPERVISORY PATENT EXAMINER